User's Guide

micro-line®

C32CPU

professional

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1. General

1.1 Introduction

The C32CPU board is a low-cost embedded system of the ORSYS micro-line® xxCPU family with modern and powerful Digital Signal Processor (DSP) and various peripheral boards. The C32CPU board operates with a Texas Instruments 32-bit floating point TMS320C32 Digital Signal Processor. The TMS320C32 processor is particularly characterized by extremely low costs combined with the high computing power of the C3x-floating point core and with an outstanding price/power ratio. The TMS320C32 processor's multiplier operates with 32 bit (floating point) or 24 bit (integer) input data. The ALU accuracy is 40 bit (floating point) or 32 bit (integer). The CPU core has furthermore a 32 bit barrel-shifter and two independent address generators in order to accomplish a parallel execution of commands with several operands. The address width is 24 bit providing an address space of 16 Mwords. The TMS320C32 processor's available clock frequencies are 40, 50 and 60 MHz.
In addition to the 0.5 Kwords of processor-internal RAM, the C32CPU board provides an external static RAM of either 32 Kwords (128 Kbytes), 128 Kwords (512 Kbytes) or 512 Kwords (2 Mbytes). Accesses to the external memory can be buffered with the TMS320C32 processor internal 64-words deep program cache memory. The external memory is available in two versions with either high speed or low power consumption. The flash-EPROM boot memory is available in the two sizes 128 Kbytes or 512 Kbytes.
Operations with ORSYS micro-line® systems are virtually problem-free. ORSYS processor boards are pin- and software compatible and categorized by price and performance. They are available with an extensive system software and universal peripheral components. ORSYS offers a powerful application end product which provides a shorter development time, low development costs and a minimum development risk.

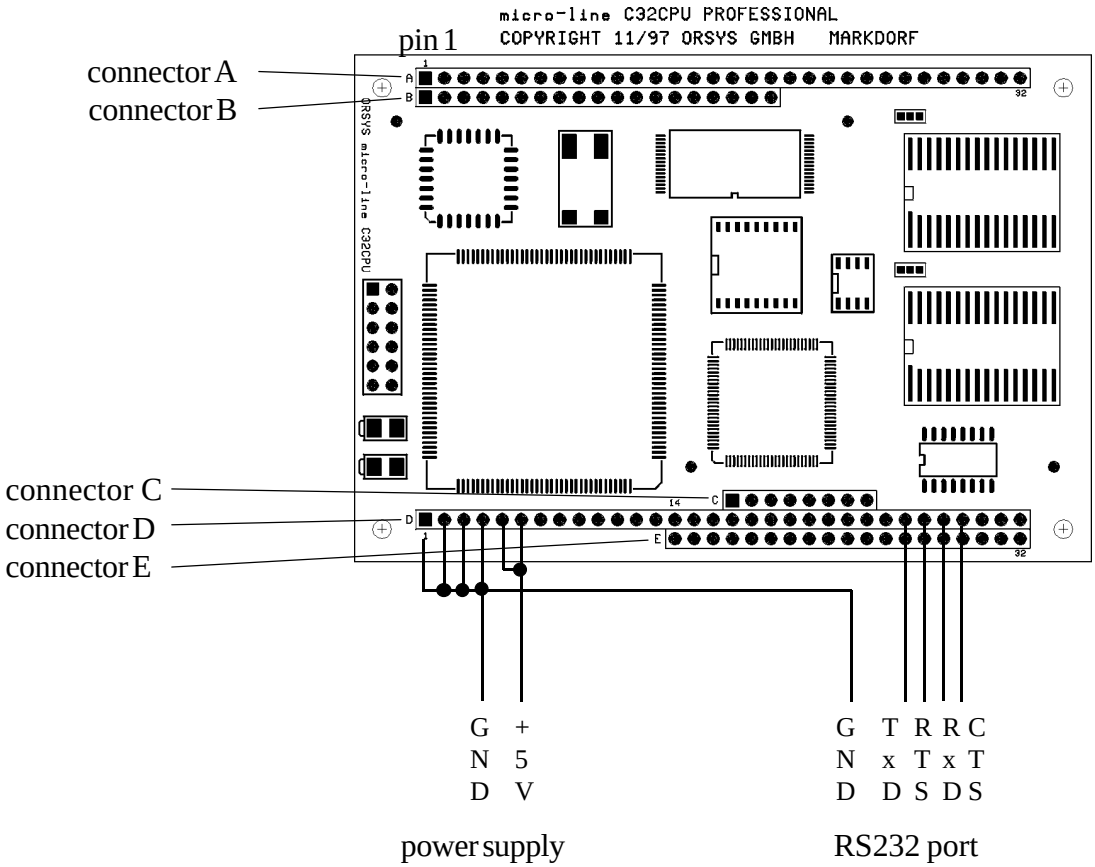
The C32CPU board low-power consumption as well as the power down modes make the use of DSP technology also highly economic for battery operated applications.

Developers always have the option to operate the processor in various modes or to use their own boot software. This is possible because the required TMS320C32 signals lead to a connector pin and all processor modes are enabled by several solder bridges. It is not necessary to have any knowledge about the processor memory map, the CPU mode or about booting in order to operate the C32CPU board.
This user's guide covers the functionalities of the C32CPU board. Details of the TMS320C32 signal processor are not discussed in this document and can be found in the Texas Instruments TMS320C32 user's guide (with reference to the TMS320C3x user's guide).

1.2 Quick Start

Prior to operating, the following FILE software has to be copied to the development PC:
DIRML.EXE, DIRML.SET, DELML.EXE, DELML.SET, RENML.EXE, RENML.SET, FORMATML.EXE, FORMATML.SET, CHKDSKML.EXE, CHKDSKML.SET, RUNML.EXE, RUNML.SET, FLOAD3X.EXE, FLOAD3X.SET, SLOAD3X.EXE and SLOAD3X.SET.

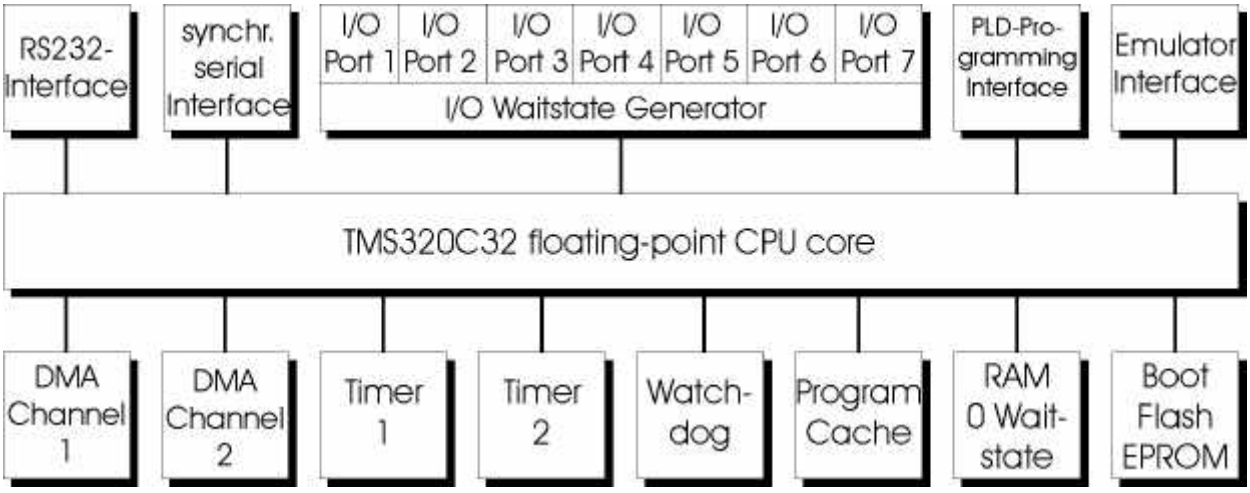
These files can be copied to an existing directory (e.g.: copy b:*.* c:\KNOWN_PATH) or a new directory can be created with the command 'md MICROLIN' (make directory). Now the files can be copied (cd MICROLIN, copy b:*.*). In order to make the programs accessible from any directory, the directory holding the files should be included in the PATH variable in the system file AUTOEXEC.BAT .
The board operates with a single 5V voltage which has to be supplied between the pins D1, D2, D3, D4 (ground) and D5, D6 (+5V). The supply voltage must not exceed 5.5 V and must not be reversed, otherwise the C32CPU board could be permanently damaged.
The development PC and the C32CPU board have to be connected via a RS232 interface. The corresponding pins on the C32CPU board are: D28 (RxD), D26 (TxD), D27 (RTS), D29 (CTS) and D1 (ground).
The pinout of the 9-pin RS232 connector is: 2 (RxD), 3 (TxD), 7 (RTS), 8 (CTS) and 5 (ground). The RS232 cable between the C32CPU board and the PC has to be a null-modem cable (TxD [PC] -> RxD [C32CPU] and upside down). The cables RTS and CTS also have to be crossed.
All necessary hardware and power supply requirements can be met by using an available low-cost micro-line® stand-alone carrier platform.



Now the power supply can be connected to the C32CPU board. The installed user program 'TOGGLE_LED' has to be booted automatically and toggle the red LED. When executing the command 'DIRML' on the development PC, the directory of the C32CPU board`s flash memory is displayed which contains the user program 'TOGGLE_LED'. The C-option of the command can be used to select the PC's COM port. The syntax is 'DIRML -Cx' (x = 1 or 2: used COM port).

2. Hardware

2.1 C32CPU Block Diagram



2.2 RS232 Interface

The RS232 interface with its integrated line drivers is used as a communication interface between the development PC and the C32CPU board. All download processes as well as all FILE operations are executed via the RS232 interface. The RS232 interface can additionally be used as an universal interface, e. g. by the Standard-I/O (TMS320-3/4xSTDI/O.LIB). Therefore, programmers are able to use functions like printf(), getch(), putch(), etc. The serial interface device is of type SCC2691. Together with C32CPU board line drivers, asynchronous transfer rates of up to 115200 baud are possible. The SCC2691 data sheet is enclosed in the appendix.
The interface consists of the signals TxD (Transmit), RxD (Receive), RTS (Request To Send) and CTS (Clear To Send).

2.3 Synchronous Serial Interface

The synchronous serial interface is integrated in the TMS320C32 processor. The TMS320C32 provides a fast, universal communication interface (up to 15 MBit/s with a 60 MHz processor) which can be used as a multi-processor communication link or as an interface to serial peripheral devices such as D/A or A/D converters. The synchronous serial interface consists of the signals DR0 (Data Receive), DX0 (Data Transmit), CLKR0 (Clock Receive), CLKX0 (Clock Transmit), FSR0 (Frame Sync Receive) and FSX0 (Frame Sync Transmit). For further information, please refer to the Texas Instruments TMS320C3x user's guide.

2.4 Port Pin Input/Output

The C32CPU board is prepared for a parallel port pin input/output function. This enables the use of external FIFOs or Latches (e.g. 74HC574) as output ports and Latches or parallel busdrivers (e.g. 74HC541) as input ports. The external devices are controlled by the signals HOST_OUT_CLK and /HOST_IN_OE . The input/output port occupies the I/O addresses from 0x810000 to 0x813FFF. The pin-timing of the two control signals HOST_OUT_CLK and /HOST_IN_OE is corresponding with the /IOSTRB signal + 1 PLD delay. An application example can be found in the appendix.

The parallel port pin input function can be used for parallel booting from a host processor via the I/O addresses 0x810000 to 0x813FFF. The signals XF0 and XF1 can be used as handshake signals. In order to set the corresponding boot configuration, several solder bridges have to be set (see paragraph 4.2).

2.5 I/O (Input/Output) port 1...7

When using the seven available I/O ports, it is possible to simultaneously and directly connect up to seven different customary peripheral devices (e.g. parallel port devices, serial port devices, timers, A/D and D/A converters, display boards, etc.) to the C32CPU board without any additional glue logic. The programable /IOSTRB waitstate generator in the TMS320C32 processor's /IOSTRB control register can compensate timing differences between the fast signal processor and the usually slower peripheral devices. The default state after reset is 7 waitstates for the entire I/O space. The two SWW-bits in the /IOSTRB control register should remain at their default values ´1 1´ .
The I/O port consists of the signal lines D0...D31 (data), A0...A18 (addresses), /CS1.../CS7 (chip select), /RD (read), /WR (write), R/W (read/write), /IOSTRB (strobe), /INT0.../INT3 (interrupt), /IACK (interrupt acknowledge), /RESETOUT (reset, active low) and RESETOUT (reset, active high). If necessary, the /IACK-output signal can be pulsed in an interrupt service routine by using the assembler command IACK.
The two signals /RD and /WR are an alternative to the signals R/W and /IOSTRB. Either signal pair can be used depending on the type and manufacturer of the peripheral device. In general, Intel compatible devices are controlled by the signals /RD and /WR and Motorola compatible devices by the signals R/W and /IOSTRB.

2.6 DMA Controllers

The two DMA (Direct Memory Access) controllers of the TMS320C32 processor enable data transfers within the C32CPU board or via any external interface (e.g. RS232 interface, I/O interface, etc). The maximum data transfer rate is 60 MByte/s for internal data transfers and 30 MByte/s for external interfaces. External DMA requests are signalled via interrupt lines. For further information, please refer to the Texas Instruments TMS320C3x user's guide.

2.7 Timer 0, Timer 1

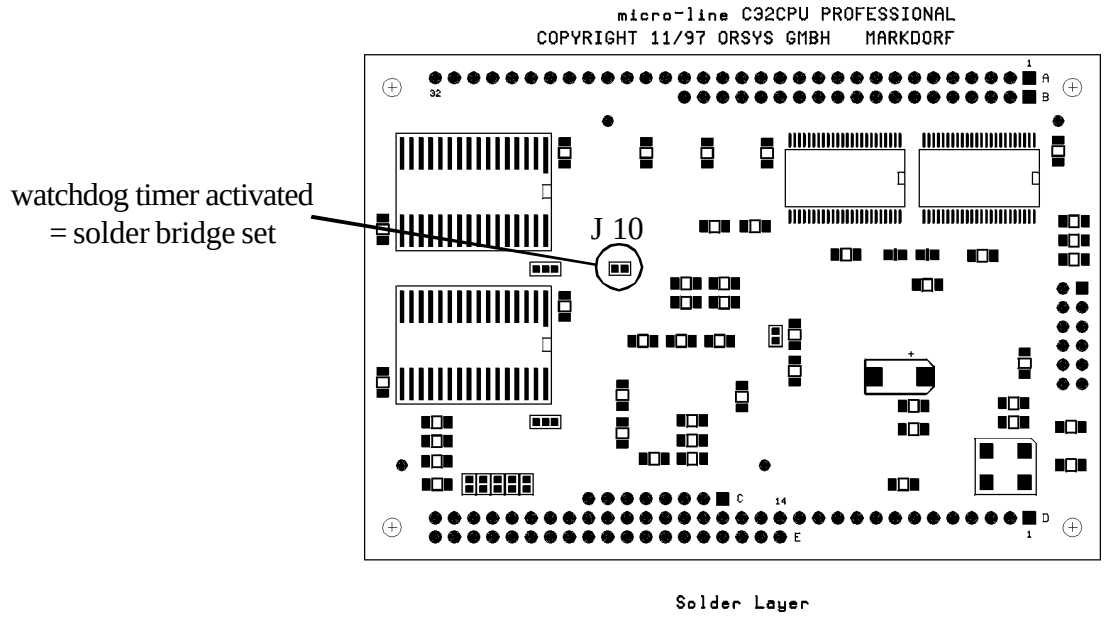
The TMS320C32 processor provides two programmable timers which can be used to generate application-specific clocks or system timings. The two signal lines TCLK0 and TCLK1 (both available on the micro-line® bus) can be configured as output signals of the corresponding timer or as timer clock inputs to count external events. For further information, please refer to the Texas Instruments TMS320C3x user's guide.

2.8 Auxiliary Timer

The SCC2691 UART device provides an additional timer. The SCC2691 timer function can be used to generate periodic system interrupts. The SCC2691 device can also be used as a serial interface.
The FILE handling of the external development PC via the SCC2691device does not interfere with the timer function and does not have to be considered when the timer is activated. The data sheets for the SCC2691 device are enclosed in the appendix.

2.9 Reset Generator, Watchdog

The C32CPU board provides a reset generator which generates a defined reset pulse during power ON, during a manual reset (e.g. with a /RESETIN pin switch), during a power supply drop below 4,65 V or in case of a watchdog event. The generated reset pulse interval lasts at least 140 ms and the lines /RESETOUT and RESETOUT are activated for 140 ms. The watchdog can be activated with solder bridge J10. If the watchdog is not required, solder bridge J10 remains open (*default state = watchdog inactive).* The maximum watchdog retrigger interval lasts 1,6 seconds. After each retrigger interval, a reset pulse is generated. The watchdog is retriggered by a read- or write access to the SCC2691device (I/O address 0x814000...0x814007).



2.10 Memory

2.10.1 RAM

The 32-bit wide organized RAM can be used as program memory and as data memory. There are several configurations of external memory available:

- 0 waitstate RAM:

  1.) 32 Kwords (128 Kbytes)
  2.) 128 Kwords (512 Kbytes)

- 55 ns low-power RAM (with waitstates):

  3.) 32 Kwords (128 Kbytes)
  4.) 128 Kwords (512 Kbytes)
  5.) 512 Kwords (2 MByte)

The number of waitstates for the 55ns RAM depends on the processor's clock speed and is between one (40 and 50 MHz) and two waitstates (60 MHz).

2.10.2 Flash-EPROM

The flash-EPROM is the system's boot memory. The flash-EPROM contains all user programs when the processor is in the bootloader mode. The flash-EPROM should **not** be read or written directly from the user program, because it is directly handled by the boot program or the FILE system software. The C32CPU board provides an integrated protection mechanism to ensure the data security of the flash-EPROM and to avoid an accidential deletion of user programs.
The flash-EPROM device permanently stores all necessary programs for booting, download operations and FILE handlings. The stored programs cannot be deleted.

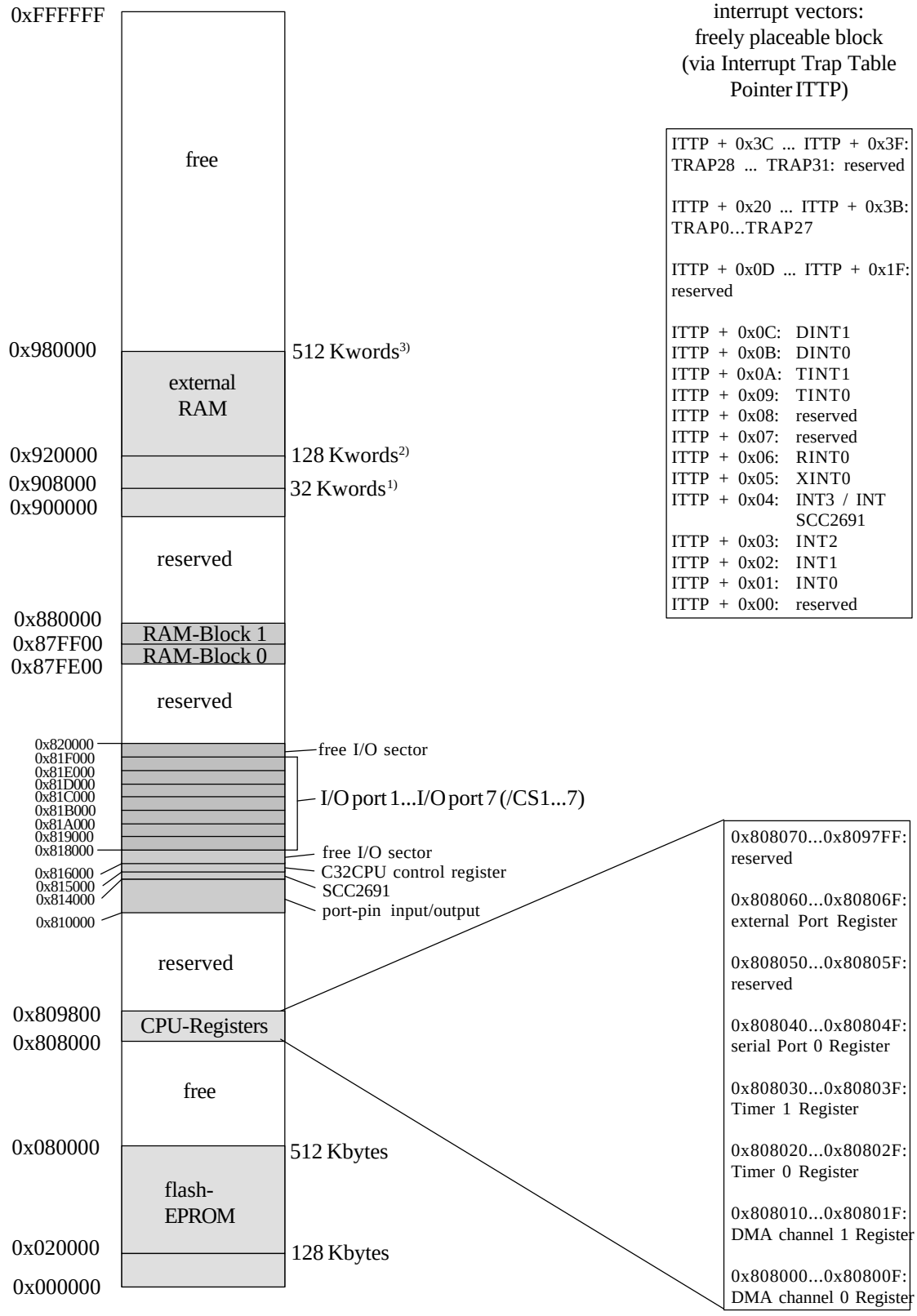
The C32CPU board supports two flash-EPROM versions:

1.) 128 kbytes
2.) 512 kbytes

2.10.3 Program Cache

The TMS320C32 processor has an integrated 64-words program cache memory to buffer instructions which were read from the external RAM. When using the program cache memory, the processor speed improves and the processor achieves optimum results for its internal parallel resources. In order to activate the cache memory, bit 11 (CE, Cache Enable) in theTMS320C32 processor status register has to be set.

2.10.4 C32CPU Memory Map



1) = 0x907E00...907FFF is reserved in the 32 Kwords RAM version

2) = 0x91FE00...91FFFF is reserved in the 128 Kwords RAM version

3) = 0x97FE00...97FFFF is reserved in the 512 Kwords RAM version

2.11 I/O Register

The complete I/O space (0x810000 to 0x81FFFF) operates with 7 waitstates after power ON. A new number of waitstates can be programmed via the three WTCNT (Waitcount) bits in the /IOSTRB control register. The two SWW (Software Wait Mode) bits of the /IOSTRB control registers should be left at their default values ´1 1´.

Port Pin Input/Output (addresses: 0x810000 to 0x813FFF):

- writing activates the /PORT_OUT_CLK pin, reading activates the PORT_IN_OE pin.

SCC2691 Register (address: 0x814000 to 0x814007)
For more information, please refer to the SCC2691 data sheet in the appendix.

MR1 (Mode Register 1) and MR2 (Mode Register 2):
- address: 0x814000
- both registers are readable and writable

SR (Status Register) and CSR (Clock Select Register):
- address: 0x814001
- SR readable, CSR writable

CR (Command Register) and Test Register 1:
- address: 0x814002
- Test Register 1 readable, CR writable

RHR (Receive Holding Register) and THR (Transmit Holding Register):
- address: 0x814003
- RHR readable, THR writable

ACR (Auxiliary Control Register) and Test Register 2:
- address: 0x814004
- Test Register 2 readable, ACR writable

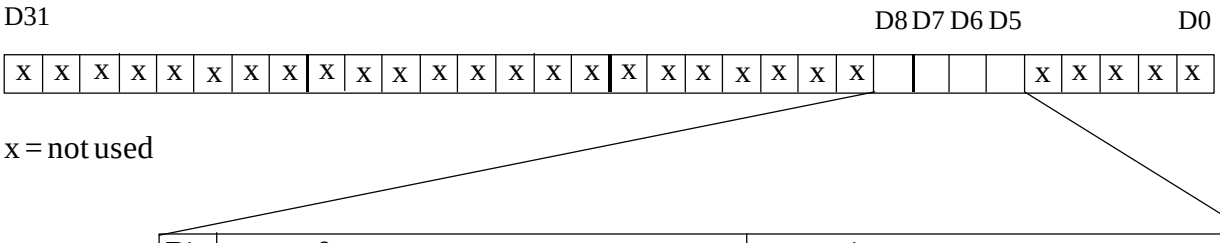
ISR (Interrupt Status Register) and IMR (Interrupt Mask Register):
- address: 0x814005
- ISR readable, IMR writable

CTU (Counter / Timer Upper) and CTUR (Counter / Timer Upper Register):
- address: 0x814006
- CTU readable, CTUR writable

CTL (Counter / Timer Lower) and CTLR (Counter / Timer Lower Register):
- address: 0x814007
- CTL readable, CTLR writable

C32CPU Control Register (address: 0x815000):

- write only



Bit	0	1
D5	*PC FILE operation locked*[1)]	PC FILE operation enabled
D6	*red LED OFF*	red LED ON
D7	*board operation*	hardware reset
D8	*RS232 driver active*	RS232 driver shutdown

- *default state after reset*

[1)] = when the PC FILE operation is locked, FILE commands can only be executed by initiating a manual reset on the C32CPU board, after invoking the requested command on the development PC (e.g. DIRML).

I/O port 1 up to I/O port 7:

- addresses: 0x818000...0x818FFF (/CS1), I/O port 1: free for external peripherals
- addresses: 0x819000...0x819FFF (/CS2), I/O port 2: free for external peripherals
- addresses: 0x81A000...0x81AFFF (/CS3), I/Oport 3: free for external peripherals
- addresses: 0x81B000...0x81BFFF (/CS4), I/O port 4: free for external peripherals
- addresses: 0x81C000...0x81CFFF (/CS5), I/O port 5: free for external peripherals
- addresses: 0x81D000...0x81DFFF (/CS6), I/O port 6: free for external peripherals
- addresses: 0x81E000...0x81EFFF (/CS7), I/O port 7: free for external peripherals

2.12 Interrupts

In addition to the processor-internal interrupt sources, the C32CPU board provides four external interrupt lines (/INT0 to /INT3) on the micro-line® bus as well as an interupt line for the onboard RS232 interface. The external interrupt lines cause an interrupt on the processor when asserted to low. The signals can be programmed as edge or level-triggered inputs.
The interrupt signal /INT3 has a double function on the C32CPU board: 1) the C32CPU board provides a corresponding pin for external hardware interrupts and 2) it is used by the onboard RS232 interface. The SCC2691 device Status Register (SR) can be polled in the interrupt service routine in order to identify the two interrupt sources.

2.13 Port Pins

Some special function pins can also be used as general-purpose digital inputs/outputs if the corresponding functionality is not needed.

Synchronous Serial Interface

All lines of the synchronous serial interface (DR0, DX0, CLKR0, CLKX0, FSR0 and FSX0) can be initialized as digital inputs or outputs.

Timer 0 and Timer 1 lines

The lines TCLK0 and TCLK1 of the TMS320C32 processor can be used as digital inputs or outputs if the external timer function is not used.

Universal lines XF0 and XF1

The signals XF0 and XF1 of the TMS320C32 processor can be used as digital inputs or outputs.

2.14 LEDs

The C32CPU board provides a red and a green LED. The green LED is used as a visual control light for accesses to the flash-EPROM device. The green LED operates similar to the LEDs found on PC hard disks and lights up simultanously with every flash memory access. The red LED is software controllable and can be switched on or off by setting or resetting Bit D6 of the C32CPU control register.

2.15 Clock Frequency / Processor Performance

The C32CPU board is available with 40, 50 and 60 MHz clock frequencies. The resulting maximum processor performance is 40, 50 and 60 MFLOPS (Million Floating Point Operations Per Second) or 20, 25 and 30 MIPS (Million Instructions Per Second).

3. Software

3.1 Summary

The C32CPU board's FILE-system consists of the commands DIRML, DELML, RENML, FORMATML, CHKDSKML, RUNML, FLOAD3X and SLOAD3X. All commands are stored as .EXE and .SET files on the development PC. Their counterparts are residently stored on the C32CPU board's flash-EPROM. In order to execute a FILE command, the command has to be entered on the development PC, using MS-DOS (3.3 or higher, or a WIN95 or WIN NT DOS Shell), e.g. DIRML. The communication to the C32CPU board uses the RS232 interface. After entering the command, the active user program on the C32CPU board is stopped, the FILE-system software is loaded and the command is executed. Finally, the active user program is restarted.
In order to select a COM port on the development PC, the command can be entered with the C-option, e.g. DIRML -Cn (n = 1 or 2). The selected COM port is stored on the development PC and automatically used for subsequent calls. The command DIRML -H or DIRML ? starts the HELP-function. The use of these parameters applies to all FILE-commands.

3.2 DIRML

The command DIRML lists the directory of the C32CPU flash-memory on the development PC with FILE name, date, time and size of the maximum 63 storable FILES. The auto booting user program and the remaining flash-EPROM memory space are additionally displayed.

3.3 DELML

The command (Delete) DELML <Name> deletes the mentioned FILE on the C32CPU board. The memory space which was occupied by the deleted FILE automatically becomes available for other FILES.

3.4 RENML

The command (Rename) RENML <OldName NewName> changes the name on the C32CPU board from (OldName) to (NewName). The maximum length of a FILE name is 15 characters.

3.5 FORMATML

The command FORMATML formats the flash-EPROM on the C32CPU board. All user programs will be deleted. The resident FILE-system is still present after a flash-formatting.

3.6 CHKDSKML

The command (Check disk) CHKDSKML checks every FILE on the flash-EPROM of the C32CPU board. The test results, the number of FILES, the overall memory size and the amount of free memory space on the flash-EPROM are displayed on the development PC screen.

3.7 RUNML

The command RUNML <Name> sets the mentioned program to the auto booting program and starts it on the C32CPU board. After each C32CPU board reset, the mentioned program is booted automatically.

3.8 FLOAD3X

The command (Flash Load) FLOAD3X is a download program, which loads a user program in Extended Tektronix-Format (created by the command: HEX30 <Name>) via RS232 into the C32CPU board. The user program will be permanently stored as a FILE with program name, date, time and program size on the C32CPU board. After loading, the program is declared to the auto booting program and started. The program will be automatically booted after each C32CPU board reset. The command FLOAD3X <Name> has to be entered on the development PC in order to start the loading process.

3.9 SLOAD3X

The command (Speed Load) SLOAD3X is a download program, which loads a user program in Extended Tektronix-Format (created by the command: HEX30 <Name>) via RS232 into the RAM of the C32CPU board. In order to start the loading process, the command SLOAD3X <Name> has to be entered on the development PC. The user program will be loaded and started. When the C32CPU board is reset or powered off, the user program is deleted on the C32CPU board.

3.10 C-Compiler, Assembler

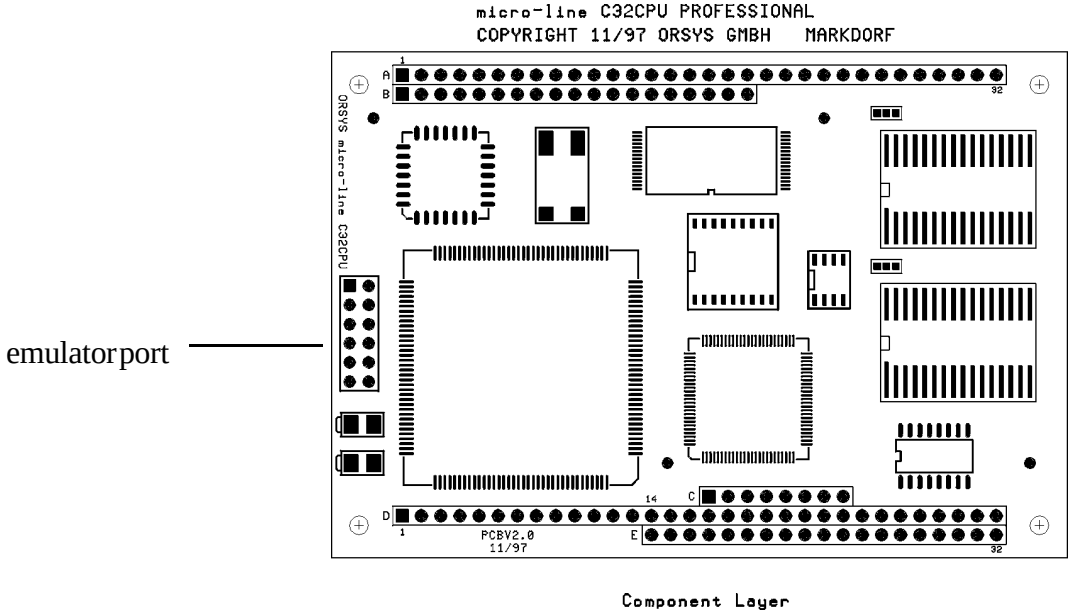
The basic development system consists of a linker and an assembler. This is sufficient to implement software projects in assembly language. The Texas Instruments (TI) order number is: TMDS3243850-02 (PC version).
An extended development system consists of an ANSI C-Compiler, Assembler and Linker. Programs can be written in 'C'- or assembly language. Inline assembly is supported as well as the integration of assembly written algorithms into a 'C'-software project. The TI order number for this package is: TMDS3243855-02 (PC version).

3.11 C++ Compiler, ADA Compiler

In addition to the above-mentioned programming languages, there are Compilers for the programming languages C++ and ADA available.

3.12 Emulator

TI as well as other Third Parties offer a choice of several emulator systems. The emulators normally consist of a PC card which is connected to the target system via an emulator cable. The emulator cable fits the emulation connector of the C32CPU board and activates the on-chip emulator. All available emulators support symbolic debugging with all important debugging functions (e.g. breakpoints, single step, display of registers, variables and memory sections, simultanous debugging of C and assembler codes, etc.) A window-based user interface facilitates the use of the emulator.



3.13 Simulator

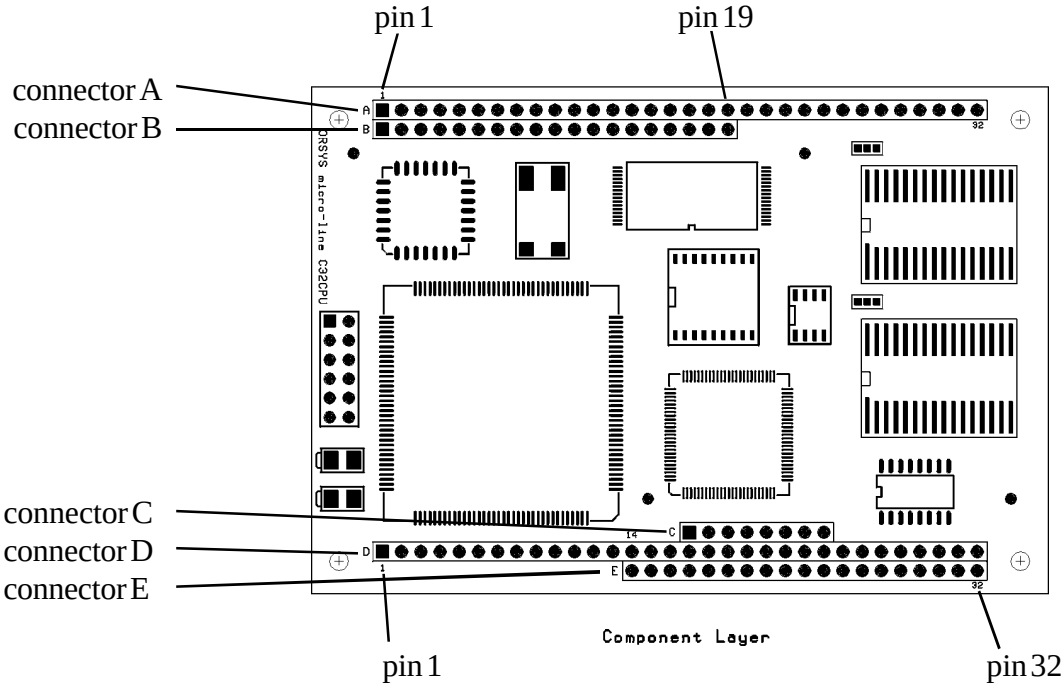
As an alternative to the emulator, software can also be tested with the TI simulator. The simulator supports the same debugging techniques as the emulator and provides the same user interface. The difference between emulator and simulator is, that when using the emulator, the software is executed on the C32CPU hardware, while the simulator merely displays a simulation of the target processor on the PC. The TI order number for the simulator package is: TMDS3245851-02 (PC version).

3.14 Real-Time Operation Systems

For larger software projects, the two real-time operation systems SPOX from SPECTRON and VIRTUOSO from EONIC SYSTEMS can be run on the C32CPU board. They are both real-time multitasking operation systems with very good results for Digital Signal Processors (DSPs). In addition to the kernel operation systems, there are different libraries available which offer mathematic functions, special DSP algorithms or enable a communication with other host operation systems (e.g. MS-DOS, Windows, LynxOS, OS-9, SunOS and VxWorks).

4. Appendix

4.1 Pin-Configuration



pin	connector A	connector B	connector C	connector D	connector E
1	D00 (I/O/Z)	A00 (O/Z)	-	GND (I)	-
2	D01 (I/O/Z)	A01 (O/Z)	-	GND (I)	-
3	D02 (I/O/Z)	A02 (O/Z)	-	GND (I)	-
4	D03 (I/O/Z)	A03 (O/Z)	-	GND (I)	-
5	D04 (I/O/Z)	A04 (O/Z)	-	+5V (I)	-
6	D05 (I/O/Z)	A05 (O/Z)	-	+5V (I)	-
7	D06 (I/O/Z)	A06 (O/Z)	-	/RESETIN (I)	-
8	D07 (I/O/Z)	A07 (O/Z)	-	/RESETOUT (O)	-
9	D08 (I/O/Z)	A08 (O/Z)	-	RESETOUT (O)	-
10	D09 (I/O/Z)	A09 (O/Z)	-	/CS1 (O)	-
11	D10 (I/O/Z)	A10 (O/Z)	-	/CS2 (O)	-
12	D11 (I/O/Z)	A11 (O/Z)	-	/CS3 (O)	-
13	D12 (I/O/Z)	A12 (O/Z)	-	/CS4 (O)	-
14	D13 (I/O/Z)	A13 (O/Z)	-	/CS5 (O)	-
15	D14 (I/O/Z)	A14 (O/Z)	-	/CS6 (O)	-
16	D15 (I/O/Z)	A15 (O/Z)	-	/CS7 (O)	PORT_OUT_CLK (O)
17	D16 (I/O/Z)	A16 (O/Z)	/IO_DATA_EN (O)	/INT0 (I)	-
18	D17 (I/O/Z)	A17 (O/Z)	/FLA_OE (I/O)	/INT1 (I)	-
19	D18 (I/O/Z)	A18 (O/Z)	/FLA_CS (I/O)	/INT2 (I)	/PORT_IN_OE (O)
20	D19 (I/O/Z)	-	/IO_DATA_DIR (O)	/INT3 (I)	DR0 (I/O/Z)
21	D20 (I/O/Z)	-	-	/IACK (O/Z)	DX0 (I/O/Z)
22	D21 (I/O/Z)	-	-	/IORD (O)	CLKR0 (I/O/Z)
23	D22 (I/O/Z)	-	-	/IOWR (O)	CLKX0 (I/O/Z)
24	D23 (I/O/Z)	-	/ISPEN (I)	R/W (O/Z)	FSR0 (I/O/Z)
25	D24 (I/O/Z)	-	-	/IOSTRB (O/Z)	FSX0 (I/O/Z)
26	D25 (I/O/Z)	-	-	TXD (O)	XF0 (I/O/Z)
27	D26 (I/O/Z)	-	-	RTS (O)	XF1 (I/O/Z)
28	D27 (I/O/Z)	-	-	RXD (I)	TCLK0 (I/O/Z)
29	D28 (I/O/Z)	-	-	CTS (I)	TCLK1 (I/O/Z)
30	D29 (I/O/Z)	-	-	/RDY (I)	CLK_3,68MHZ (O)
31	D30 (I/O/Z)	-	-	/HOLD (I)	H1 (O)
32	D31 (I/O/Z)	-	-	/HOLDA (O/Z)	/SHZ (I)

4.1.1 Pin-Description

Connector A:

D00...D31:
These are the bidirectional data lines of the TMS320C32 processor. During reset or when another busmaster is driving the bus, the lines are switched to high impedance state or to inputs. The data lines D00...D15 are buffered by bidirectional bus drivers on the C32CPU board. The external data lines D00...D15 remain high impedance during local onboard memory accesses. They only become active during I/0 accesses. The data lines D16...D31 are directly connected to the TMS 320C32 processor.

Connector B:

A00...A18:
These are the address lines of the TMS320C32 processor. They are outputs during normal processor operation. During reset or when another busmaster is driving the bus, the lines are switched to high impedance state or to inputs. The address lines A00...A13 are buffered by bus drivers on the C32CPU board. In case of a local onboard memory access, A00...A13 remain high impedance. They only become active during I/O accesses. A14...A18 are directly connected to the TMS320C32 processor.

Connector C:

/IO_DATA_EN:
Active low, output. If used, the data lines D16...D31 should be buffered externally on a specific system board. For this purpose, the driver SN74ABT16245 is recommended. The signal /IO_DATA_EN has to be connected to the data-driver output enable pins. The signal /IO_DATA_EN enables the driver during every access to the I/O adresses 810000h to 81FFFFh. Note: If external bus drivers are used, they should be located as near as possible to the board bus pins. A maximum line length of 10 cm (about 4 inches) should not be exceeded. Enough distance between the bus lines should be kept in order to keep capacitive coupling between them as low as possible. The ground and the +5V power supply of the bus drivers should be well decoupled by 100nF capacitors. The power supply on the bus drivers system board should be realized as copper planes. The planes have to be connected to the digital ground and the +5V pins of the micro-line® bus.

/FLASH_OE:
Output Enable line (active low, output) of the onboard flash-memory device. /FLASH_OE is usually not required.

/FLASH_CS:
Chip Select line (active low, output) of the onboard flash memory device. /FLASH_CS is usually not required.

/IO_DATA_DIR:
Active low, output. If used, the data lines D16...D31 should be buffered externally. For this purpose, the driver SN74ABT16245 is recommended. The signal /IO_DATA_DIR has to be connected to the data-driver direction pins. The driver side A should be connected to the processor board side and the driver side B should be connected to the external peripherals.

/ISPEN:
Program pin for the PLD device on the 32CPU board (active low, input). This signal always should remain unconnected.

Connector D:

GND:
Power supply: ground

+5V:
Power supply: +5V. When the voltage drops below +4.65V, the reset signal on the board is asserted. The maximum allowed voltage is +5.5V.

/RESETIN:
Reset input line (active low) for an external reset button. The signal does not have to be debounced. The C32CPU board provides an integrated pullup resistor.

/RESETOUT:
Reset output line (active low, no open collector) for external peripheral devices. The signal will be activated if the C32CPU board is reset.

RESETOUT:
Inverted /RESETOUT output signal (active high, no open collector).

/CS1:
Chip Select output (active low) of I/O port 1. /CS1 will be activated during read or write accesses to the I/O address space 0x818000 to 0x818FFF. The signal is valid during the valid address of the processor. One PLD pin-to-pin signal delay should be noticed between address valid time and /CS1 time.

/CS2:
Chip Select output (active low) of I/O port 2. /CS2 will be activated during read or write accesses to the I/O address space from 0x819000 to 0x819FFF. The signal is valid during the valid address of the processor. One PLD pin-to-pin signal delay should be noticed between address valid time and /CS2 time.

/CS3:
Chip Select output (active low) of I/O port 3. /CS3 will be activated during read or write accesses to the I/O adress space 0x81A000 to 0x81AFFF. The signal is valid during the valid address of the processor. One PLD pin-to-pin signal delay should be noticed between address valid time and /CS3 time.

/CS4:
Chip Select output (active low) of I/O port 4. /CS4 will be activated during read or write accesses to the I/O address space 0x81B000 to 0x81BFFF. The signal is valid during the valid address of the processor. One PLD pin-to-pin signal delay should be noticed between address valid time and /CS4 time.

/CS5:
Chip Select output (active low) of the I/O port 5. /CS5 will be activated during read or write accesses to the I/O adress space 0x81C000 to 0x81CFFF. The signal is valid during the valid address of the processor. One PLD pin-to-pin signal delay should be noticed between address valid time and /CS5 time.

/CS6:
Chip Select output (active low) of I/O port 6. /CS6 will be activated during read or write accesses to the I/O address space 0x81D000 to 0x81DFFF. The signal is valid during the valid address of the processor. One PLD pin-to-pin signal delay should be noticed between address valid time and /CS6 time.

/CS7:
Chip Select output (active low) of I/O port 7. /CS7 will be activated during read or write accesses to the I/O adress space 0x81E000 to 0x81EFFF. The signal is valid during the valid address of the processor. One PLD pin-to-pin signal delay should be noticed between address valid time and /CS7 time.

/INT0.../INT3:
Interrupt input lines (active low) of the TMS320C32 processor. All four interrupt inputs can be either edge or level triggered depending on the interrupt configuration bits in the TMS320C32 processor status register ST. Every interrupt line has a pullup resistor and is equipped with the necessary logic for bootmode/operation mode settings.

/IACK:
Interrupt Acknowledge output signal (active low) of the TMS320C32 processor. This line can be pulsed by the IACK instruction at an interrupt service routine.

/IORD:
I/O Read signal (output, active low). The signal is always in low impedance state and cannot be switched into tristate. /IORD is activated during a read access of the TMS320C32 processor. The timing of /IORD is equivalent to /IOSTRB + one PLD pin-to-pin signal delay.

/IOWR:
I/O Write signal (output, active low). The signal is always in low impedance state and cannot be switched into tristate. /IOWR is activated during a write access of the TMS320C32 processor. The timing of /IOWR is equivalent to /IOSTRB + one PLD pin-to-pin signal delay.

R/W:
Read/Write output signal of the TMS320C32 processor. If the signal is high, an external read cycle occurs; if the signal is low, an external write cycle occurs. During reset or when another busmaster is driving the bus, the line is switched to high impedance state or to input. The R/W signal is buffered by a bidirectional bus driver on the C32CPU board.

/IOSTRB:
I/O Strobe output (active low) of the TMS320C32 processor. The /IOSTRB signal indicates an external I/O read or write access. During reset or when another busmaster is driving the bus, the line is switched to high impedance state or to input. The /IOSTRB signal is buffered on the C32CPU board.

TXD:
Transmit Data output of the RS232 interface. The necessary $\pm$ 10V line drivers are integrated on the C32CPU board.

RTS:
Request To Send output of the RS232 interface. The necessary $\pm$ 10V line drivers are integrated on the C32CPU board.

RXD:
Receive Data input of the RS232 interface. The necessary $\pm$ 10V line drivers are integrated on the C32CPU board.

CTS:
Clear To Send input of the RS232 interface. The necessary $\pm$ 10V line drivers are integrated on the C32CPU board.

/RDY:
External Bus Ready input signal (active low). This signal can be used to insert additional hardware waitstates during external bus cycles. When additional waitstates are requested by setting /RDY to '1', the external bus cycle is extended until the /RDY signal becomes active again (´0´). The pin remains unconnected if no hardware-generated waitstates are required. The C32CPU board provides an integrated pull-down resistor.

/HOLD:
Bus Hold input signal (active low). This signal is activated by an external bus master which requests control over the C32CPU bus. This stops running software on the board-memory but it does not affect software running on the on-chip TMS320C32 processor memory. The C32CPU board provides an integrated pullup resistor.

/HOLDA:
Bus Hold acknowledge output signal (active low). The signal is asserted by the TMS320C32 processor to indicate that the C32CPU bus is switched into high impedance state in response to an activated /HOLD input signal. The C32CPU board provides an integrated pullup resistor.

Connector E:

PORT_OUT_CLK:
Port Out Clock signal (output, active low) The timing of PORT_OUT_CLK is equivalent to /IOSTRB + one PLD pin-to-pin signal delay. This signal can be used to rising-edge trigger an external Latch or a FIFO-device in transmit direction.

/PORT_IN_OE:
Port In Output Enable signal (output, active low) The timing of /PORT_IN_OE is equivalent to /IOSTRB + one PLD pin-to-pin signal delay. This signal can be used to control an external bus driver, a Latch or a FIFO-device in receive direction.

DR0:
Data Receive signal of the synchronous serial interface of the TMS320C32.

DX0:
Data Transmit signal of the synchronous serial interface of the TMS320C32.

CLKR0:
Clock Receive signal of the synchronous serial interface of the TMS320C32.

CLKX0:
Clock Transmit signal of the synchronous serial interface of the TMS320C32.

FSR0:
Frame Sync Receive signal of the synchronous serial interface of the TMS320C32.

FSX0:
Frame Sync Transmit signal of the synchronous serial interface of the TMS320C32.

XF0, XF1:
External Flag pins of the TMS320C32 processor. These lines can be used as universal I/O lines or as external hardware flags for multiprocessor interlock instructions.

TCLK0, TCLK1:
Timer Clock pins of the TMS320C32 processor. These lines can be used as outputs to create external clock signals with the internal timers or as inputs for counting external events.

CLK_3,68MHz:
3,6864 MHz clock output signal of the SCC2691 device. This clock will be stopped if the SCC2691 device is switched into the power down mode.

H1:
Bus clock output signal of the TMS320C32 processor. The frequency is half of the C32CPU board oscillator clock frequency.

/SHZ:
Shut down High Z signal (input, active low). This signal switches all TMS320C32 processor output drivers into the high impedance state and is used for testing the system. The required pullup resistor is integrated on the C32CPU board. The signal should always be left unconnected.

4.2 Alternative Processor and Boot Modes, Memory Chip Size

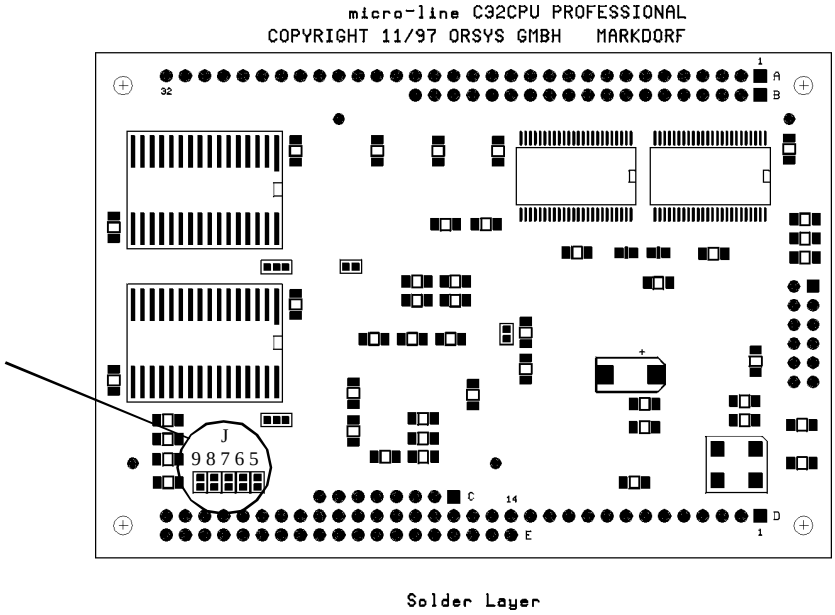
There are several boot alternatives if the integrated bootloader is not used:

4.2.1 Port-In Booting from an External Host Processor (with an external Latch or FIFO-device controlled by PORT_IN_OE):

solder bridges J9 and J8 open

to activate port-in booting :
- solder bridge J7 set and
J6 open

to enable XF0/XF1 handshake:
- solder bridges J7 and J6 set

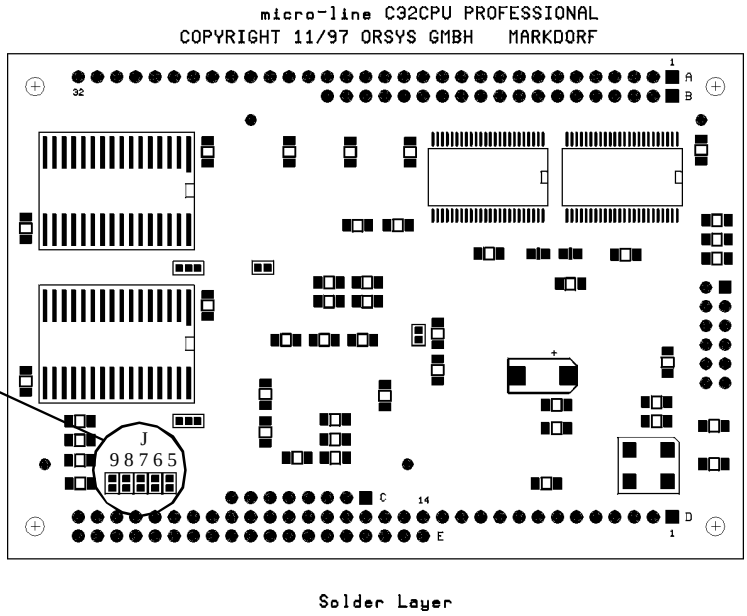


After modification of the solder bridges J6 to J9, the board can be booted via the port-in interface by the same protocol used in the 8-bit EPROM booting mode (see TMS320C32 user´s guide). It is important to construct a Rx Buffer Full/Tx Buffer Empty handshake between the host processor and the C32CPU board. The signals XF0 and XF1 can be used as handshake signals (see TMS320C32 user´s guide). To activate the handshake function, solder bridges J6 and J7 have to be set.
The maximum block size for port-in boot sequences is 16 Kbytes (4000HEX). Should the program which has to be booted be larger, a short user program loader has to be booted first, which in a second step boots the user program in full length without read-address increments (automatically made by the TI bootstrap loader) by an external host processor.
To initialize the C32CPU system, the first instruction of the loaded program has to be a dummy read cycle from address 0x1000.

4.2.2 Booting via Synchronous Serial Interface:

to activate serial interface booting :

- solder bridges J7, J8, J9 open
- solder bridge J6 set

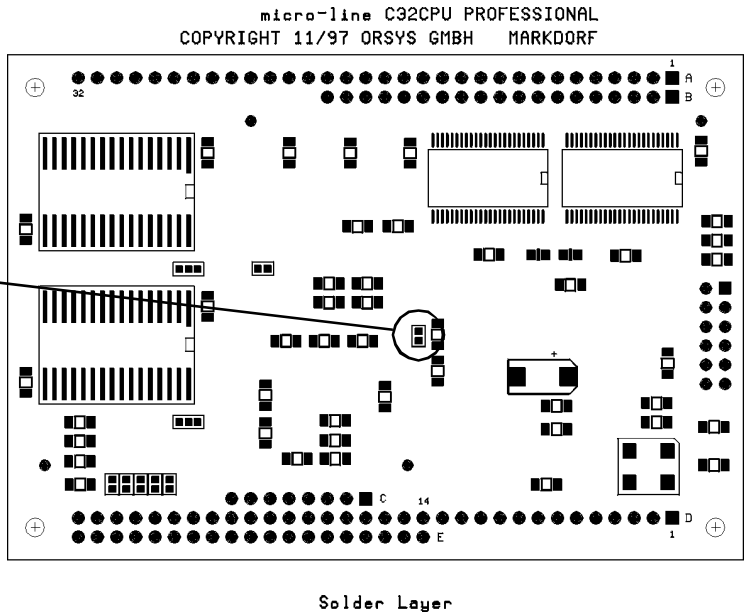


The solder bridges J6 and J9 have to be modified in order to boot the board from a host DSP via the synchronous serial interface. To initialize the C32CPU system, the first instruction of the loaded program has to be a dummy read cycle from address 0x1000. Further information about serial booting is provided in the TMS320C32 user's guide.

4.2.3 TMS320C32 Processor Operation in the Microprocessor Mode

microprocessor mode:

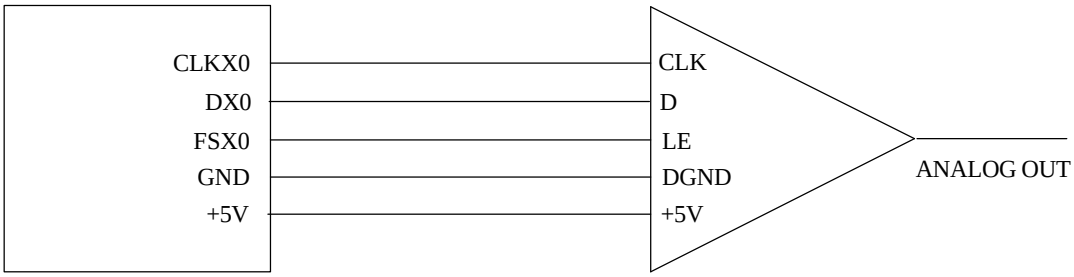
- solder bridge J14 set



The C32CPU board is in microcomputer/bootloader mode by default. It can also be run in microprocessor mode after modification of solder bridge J14. Usually, J14 should not be modified. Detailed information about the operating mode is provided in the TMS320C32 user's guide.

4.3 Application Examples

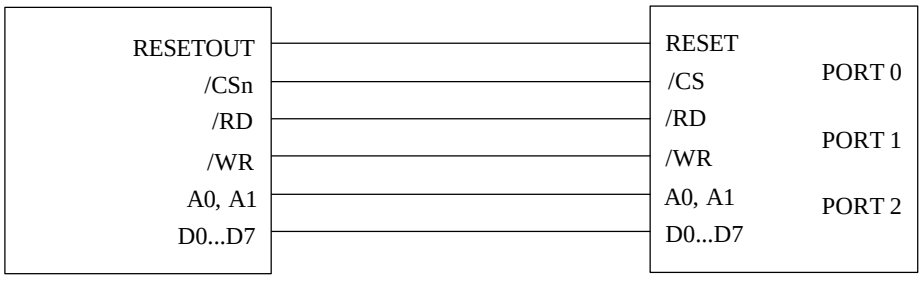
4.3.1 D/A-Converter Connecting via Synchronous Serial Interface



C32CPU board e.g. AD 1862

The C32CPU board clock output CLKX0 of the synchronous serial interface has to be connected to the AD1862 clock input. The data transmit pin DX0 has to be connected to data input D of the digital analog converter. The frame sync signal FSX0 of the serial interface has to be connected to the AD1862 Latch input LE.
By using the same method, a serial A/D converter can be connected to the C32CPU board. In this case, a timer signal can optionally be used as a start of conversion pulse. The D/A- and A/D converters can simultaneously operate at the same port, provided that the same clock is used for both converters.

4.3.2 Connecting a Parallel Port Device 82C55 via an I/O Port

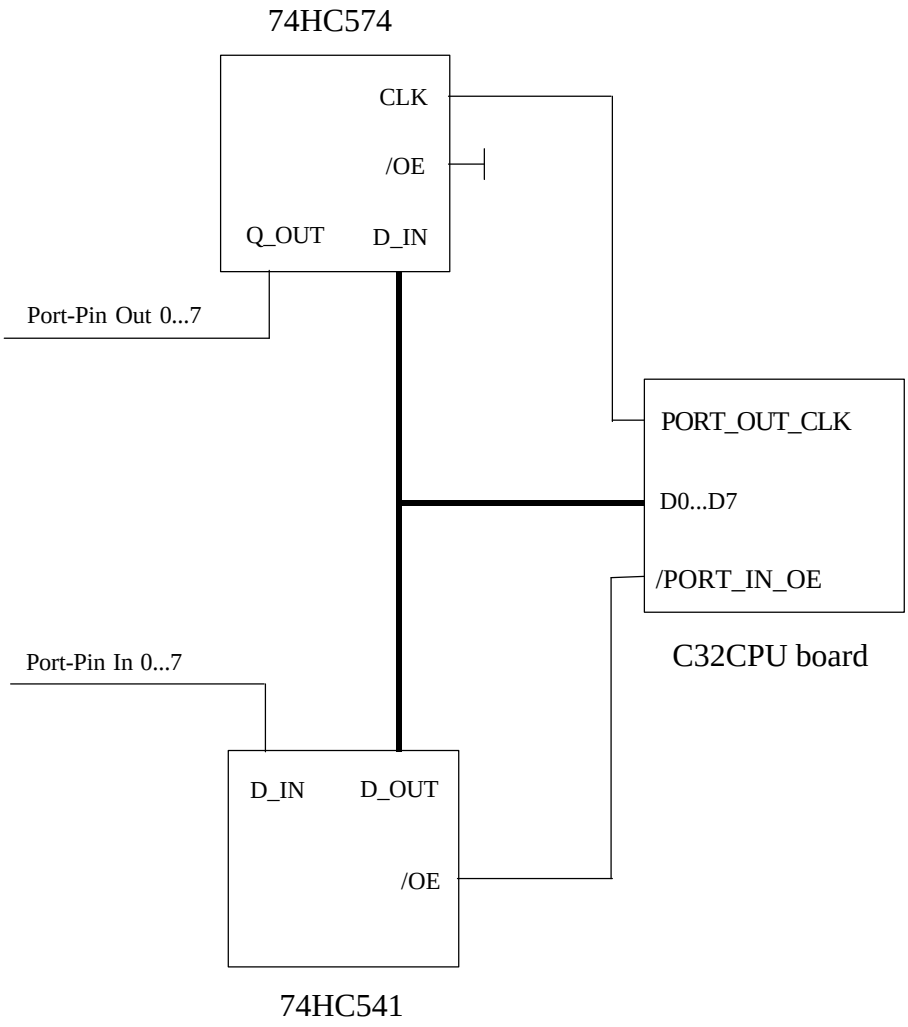


C32CPU board 82C55

The connection of a 82C55 parallel port device is shown as an example for using a customary peripheral device together with the C32CPU board. For the 82C55, the ´1´active RESETOUT signal of the C32CPU board has to be used because the 82C55 reset input signal is also ´1´active. The C32CPU board interrupt inputs /INT0 to /INT3 are not used in this case since the 82C55 has no interrupt outputs.

4.3.3 The Port-Pin In/Out Function

The Port-Pin In/Out function can be implemented by using the signals HOST_OUT_CLK and /HOST_IN_OE. The shown external devices are an 8-bit Latch 74HC574 and an 8-bit bus driver 74HC541. As an alternative to the 74HC541, a second Latch device 74HC574 can be used to build a temporary buffer (e.g. for booting). Asynchronous FIFO devices can also be used as buffer memories.



4.4 Further Remarks

4.4.1 Important Notes to External Hardware Configurations

Due to the high clock frequencies and the fast transients on the C32CPU board, the following rules always have to be observed when connecting external hardware components:

- External buses and fast control lines should not be longer then 15 cm (6 inches). Undriven external buses should not be longer then 5 cm (2 inches).
- The power supply for the micro-line® board should produce a very stable voltage. The voltage regulation of the power supply must be spikefree and HF-stable.
- The external power supply and ground should be implemented as copper planes. **Important:** Connections between the supply and ground planes as well as the peripheral devices have to be short, thick and decoupled with a capacitor of about 100 nF (to +5V)! In case of an experimental bread board, the ground wires should be at least 1,5 mm^2 thick. The basic rule is the thicker and shorter, the better.
- When connecting noise sensitive A/D or D/A converters, the layout of analog and digital ground has to follow the instructions provided by converter data sheet.
- When peripheral connections use the unbuffered data lines D16 to D31 or some of the unbuffered address lines A14 to A18, they should be driven by external bus drivers. They should be located as near as possible to the micro-line® bus. For this purpose, the drivers SN74ABT16245 or SN74ABT245 are recommended. The signal /IO_DATA_EN should be used for the output enable pins of the data drivers. The signal /IO_DATA_DIR should be used for the data driver direction pins. The address driver can be enabled permanently to drive the bus outside the C32CPU board.

4.4.2 Signal Loads

The guidelines below apply to all fast processor signals (D0...D15, A0...A13, R/W, /IOSTRB, /RD, /WR and H1):

- typical loads are about 80 pF
- loads above 160 pF should be avoided

All unbuffered bus signals (D16... D31 and A14...A18 should not be loaded beyond 40 pF. All other C32CPU board signals should not drive more then 200 pF.

4.4.3 Ambient Temperature

storage temperature: -25...+85^{0}C
operation temperature: 0...70^{0}C

operation: -25...+85^{0}C industrial temperature versions are also available.

4.4.4 Power Consumption

The C32CPU board power consumption depends very much on how frequently the external RAM is accessed. The power consumption can be reduced by activating the Power Down Modes of the SCC2691 device (see SCC2691data sheet) and of the RS232 driver (C32CPU Control Register). The TMS320C32 processor supports two Power Down Modes which reduce the performance or temporarily stop the system (see TMS320C32 user´s guide). In general, the Power Down Modes can be used to reduce the power consumption during pauses between subsequent data bursts.
Board versions with double low power 55ns-RAM (1...2 waitstates) which further reduce the average power consumption are available for applications with extremely low power consumption requirements.

clock frequency	TMS320C32 LOWPOWER-mode[1)]	only internal memory accesses MAXSPEED[2)]	all memory accesses external: 32 Kwords 0 WS RAM [2) 3) 4)]	external: 32 Kwords 55ns RAM [2) 3) 4) 5)]
40 MHz	about 30 mA	about 140 mA	about 330 mA	about 190 mA
50 MHz	about 35 mA	about 150 mA	about 350 mA	about 210 mA
60 MHz	about 40 mA	about 160 mA	about 370 mA	about 230 mA

[1)] = only internal memory accesses; processor clock = 1/16 (LOWPOWER mode); SCC2691 and RS232 driver in power down mode

[2)] = maximum system speed; SCC2691 and RS232 driver active

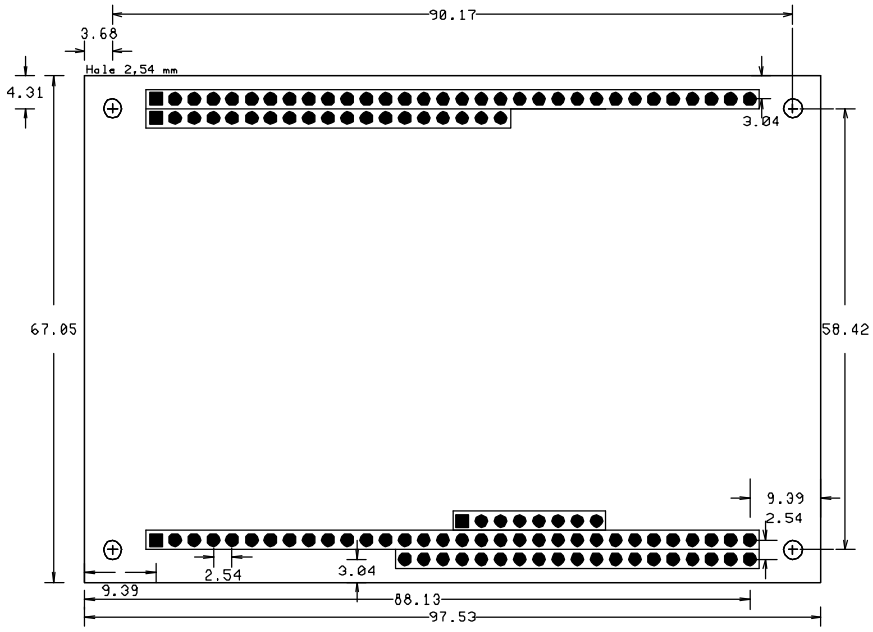
[3)] = with 128 Kwords RAM, an additional power consumption of about 10 % has to be considered

[4)] = TMS320C32 cache memory inactive; program and data are in the external RAM of the board

[5)] = with 512 Kwords RAM, an additional power consumption of about 25 % has to be considered

4.4.5 Board Dimensions

All dimensions are provided in millimeters.



The position of the four holes is symmetrical to the edges of the C32CPU board. Therefore, only one dimension is provided at the top left edge.
The position of the connectors is also symmetrical. The horizontal distance between pin 1 of the connectors and the C32CPU board's outer line and the distance between pin 32 of the connectors and the C32CPU board's outer line is always 9,39 mm.